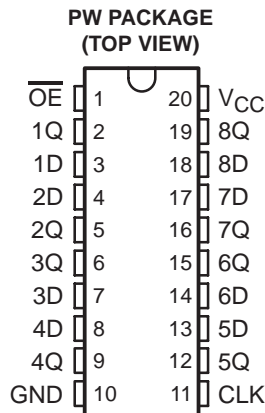


SN74LV374A-Q1

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- **Qualified for Automotive Applications**
- **Typical V_{OLP} (Output Ground Bounce)**
 $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 $>2.3\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



description/ordering information

The SN74LV374A is an octal edge-triggered D-type flip-flop designed for 2-V to 5.5-V V_{CC} operation.

This device features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION†

| T_A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| –40°C to 105°C | TSSOP – PW | Tape and reel | SN74LV374ATPWQR1 | LV374ATQ |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN74LV374A-Q1

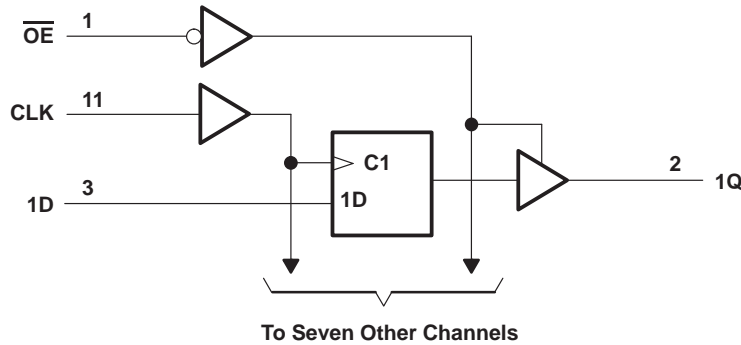
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|-----|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | -0.5 V to 7 V |
| Output voltage range, V_O (see Notes 1 and 2) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±35 mA |
| Continuous current through V_{CC} or GND | ±70 mA |
| Package thermal impedance, θ_{JA} (see Note 3) | 83°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT | |
|---------------------|------------------------------------|---|---------------------|----------|---|
| V_{CC} | Supply voltage | 2 | 5.5 | V | |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | V | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.7$ | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.7$ | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | 0.5 | V | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.3$ | | |
| V_I | Input voltage | 0 | 5.5 | V | |
| V_O | Output voltage | High or low state | 0 | V_{CC} | V |
| | | 3-state | 0 | 5.5 | |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | -50 | mA | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | -2 | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | -8 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | -16 | | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | 50 | mA | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 2 | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 8 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 16 | | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 200 | ns/V | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 100 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 20 | | |
| T_A | Operating free-air temperature | -40 | 105 | °C | |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|---|--------------|----------------|-----|---------|---------------|
| V_{OH} | $I_{OH} = -50\ \mu\text{A}$ | 2 V to 5.5 V | $V_{CC} - 0.1$ | | | V |
| | $I_{OH} = -2\ \text{mA}$ | 2.3 V | 2 | | | |
| | $I_{OH} = -8\ \text{mA}$ | 3 V | 2.48 | | | |
| | $I_{OH} = -16\ \text{mA}$ | 4.5 V | 3.8 | | | |
| V_{OL} | $I_{OL} = 50\ \mu\text{A}$ | 2 V to 5.5 V | | | 0.1 | V |
| | $I_{OL} = 2\ \text{mA}$ | 2.3 V | | | 0.4 | |
| | $I_{OL} = 8\ \text{mA}$ | 3 V | | | 0.44 | |
| | $I_{OL} = 16\ \text{mA}$ | 4.5 V | | | 0.55 | |
| I_I | $V_I = 5.5\ \text{V or GND}$ | 0 to 5.5 V | | | ± 1 | μA |
| I_{OZ} | $V_O = V_{CC}\ \text{or GND}$ | 5.5 V | | | ± 5 | μA |
| I_{CC} | $V_I = V_{CC}\ \text{or GND, } I_O = 0$ | 5.5 V | | | 20 | μA |
| I_{off} | $V_I\ \text{or } V_O = 0\ \text{to } 5.5\ \text{V}$ | 0 | | | 5 | μA |
| C_i | $V_I = V_{CC}\ \text{or GND}$ | 3.3 V | | 2.9 | | pF |



SN74LV374A-Q1

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| | | T _A = 25°C | | MIN | MAX | UNIT |
|-----------------|---------------------------------|-----------------------|-----|-----|-----|------|
| | | MIN | MAX | | | |
| t _w | Pulse duration, CLK high or low | 5 | | 5.5 | | ns |
| t _{su} | Setup time, data before CLK↑ | 4.5 | | 4.5 | | ns |
| t _h | Hold time, data after CLK↑ | 2 | | 2 | | ns |

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| | | T _A = 25°C | | MIN | MAX | UNIT |
|-----------------|---------------------------------|-----------------------|-----|-----|-----|------|
| | | MIN | MAX | | | |
| t _w | Pulse duration, CLK high or low | 5 | | 5 | | ns |
| t _{su} | Setup time, data before CLK↑ | 3 | | 3 | | ns |
| t _h | Hold time, data after CLK↑ | 2 | | 2 | | ns |

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------|-----------------|-------------|------------------------|-----------------------|------|-----|-----|------|------|
| | | | | MIN | TYP | MAX | | | |
| f _{max} | | | C _L = 50 pF | 55 | 110 | | 50 | | MHz |
| t _{pd} | CLK | Q | | 8.3 | 16.2 | | 1 | 18.5 | ns |
| t _{en} | \overline{OE} | Q | | 7.7 | 14.5 | | 1 | 17.5 | |
| t _{dis} | \overline{OE} | Q | | 5.9 | 14 | | 1 | 16 | |
| t _{sk(o)} | | | | | 1.5 | | | | |

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------|-----------------|-------------|------------------------|-----------------------|------|-----|-----|------|------|
| | | | | MIN | TYP | MAX | | | |
| f _{max} | | | C _L = 50 pF | 85 | 170 | | 75 | | MHz |
| t _{pd} | CLK | Q | | 5.9 | 10.1 | | 1 | 13.5 | ns |
| t _{en} | \overline{OE} | Q | | 5.5 | 9.6 | | 1 | 13 | |
| t _{dis} | \overline{OE} | Q | | 4 | 8.8 | | 1 | 10 | |
| t _{sk(o)} | | | | | 1 | | | | |



SN74LV374A-Q1
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

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noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------|--|------|------|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.6 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.5 | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 2.9 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

NOTE 5: Characteristics are for surface-mount packages only.

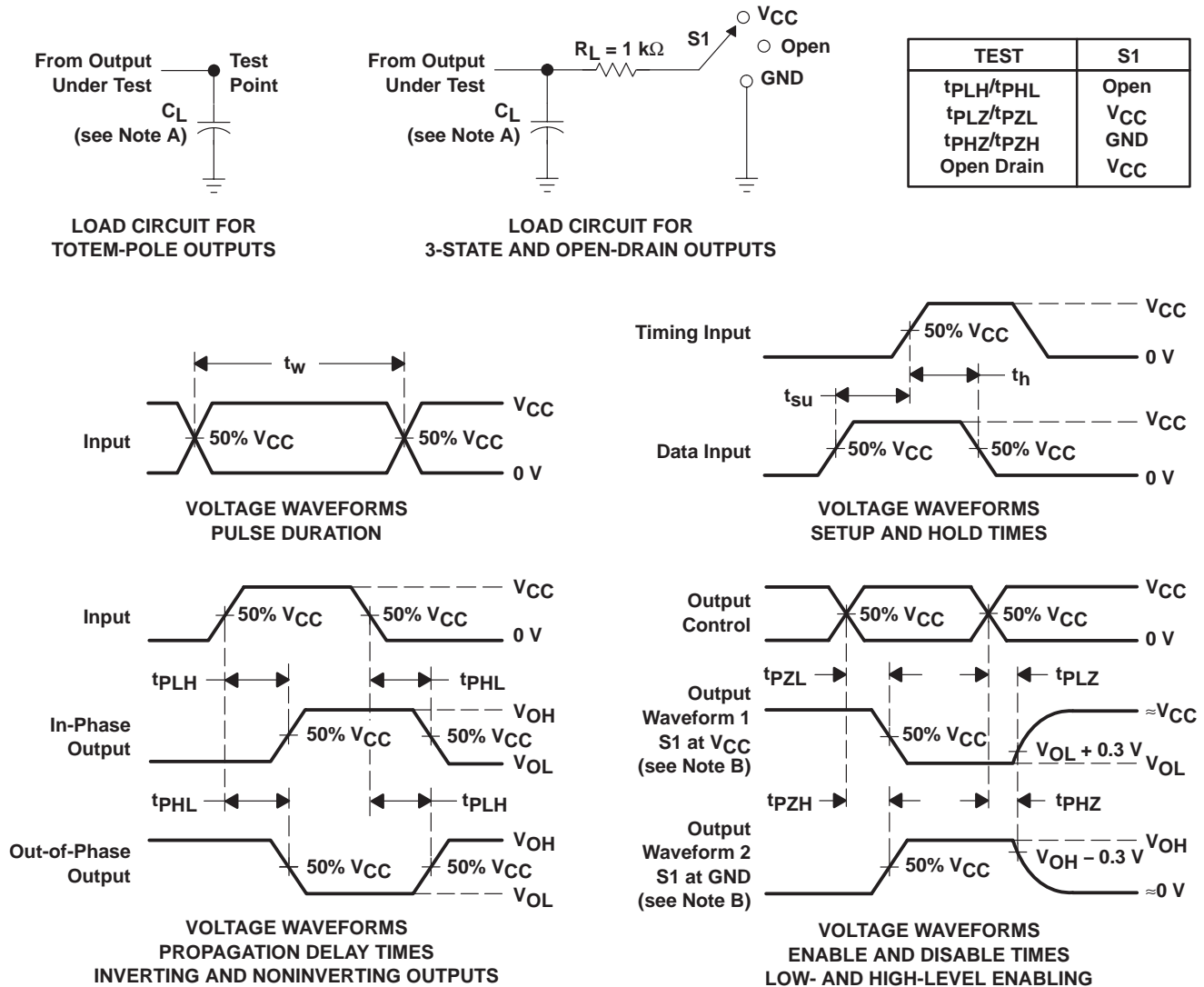
operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | V_{CC} | TYP | UNIT | |
|-----------|-------------------------------|-----------------|--|-------|------|----|
| C_{pd} | Power dissipation capacitance | Outputs enabled | $C_L = 50\text{ pF}$, $f = 10\text{ MHz}$ | 3.3 V | 21.1 | pF |
| | | | | 5 V | 22.8 | |

SN74LV374A-Q1 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LV374ATPWRG4Q1 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LV374ATPWRQ1 | ACTIVE | TSSOP | PW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Enhanced Product: [SN74LV374A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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